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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,339	ANDO, YOSHIYUKI	
	Examin r	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18, 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species of the claimed invention:

Species A consists of claims 1-18 and 21 read on figure 11

Species B consists of claims 19-20 read on figure 15.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, there is no generic claim.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

2. During a telephone conversation with attorney Richard D. Fuerle (Reg. No. 24,640) on 12/19/2003 a provisional election was made with traverse to prosecute the invention of species A, claims 1-18 and 21. Affirmation of this election must be made by applicant in replying to this Office action. Claims 19-20 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Objections

1. Claims 14 and 15 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In this instant, claims 14 -15 define the usage of the complementary source follower circuit in and LSI therefore fail to further limit the complementary source follower circuit of claim 1.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 12-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 12-13 are indefinite because they are method claims dependent upon apparatus claim 1.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-18 and 21 are rejected under 35USC 103(a) as being unpatentable over Dingwall (USP 4,354,151) in view of Yamauchi et al. (USP 6,373,321). Figure 3 of Dingwall shows complementary source follower circuit comprising N and P channel transistors (N2 and P2) coupled in series between first and second power supply (Vdd and ground), each transistor has a gate, source, drain and back gate terminal. Dingwall does not show a back bias control circuit coupled to the back gate terminals of the transistors for controlling the threshold voltage of the transistors in active and standby modes as called for in claims 1 and 16. Figures 1A and AB of Yamauchi et al. show CMOS buffer circuit comprising P and N channel connected in series between a power supply and ground. The back gate of the P and N channel are controlled by a back bias control circuit (shown in figure 1c). The back bias control circuit supplies the back gate terminal of the transistors with different bias potentials in active and standby mode thus varies the threshold voltage of the transistors accordingly. Specifically, the threshold voltage of the transistor is lowered in the active mode than in the standby mode to minimize the leakage current flow between source and the substrate thus reducing power consumption. Therefore, it would have been obvious to person skilled in the art at the time the invention was

made to include the Yamauchi et al.'s back bias control circuit in the circuit arrangement of Dingwall for controlling the threshold voltage of the N and P channel transistors thus reducing power consumption.

3. Regarding claims 2-6, 17-18 and 21, figures 2A-2B, 4 and 5 of Yamauchi et al. further teaches that CMOS transistor can also be fabricated in N, P or SOI substrates. The variations between these mythologies are well known in the art therefore it will not be patentable under 35USC 103(a).

4. Regarding claim 7, the input signal applied to the combined source follower circuit of Dingwall and Yamauchi can also an analog signal.

5. Regarding claim 8, the level shifter is seen as transistors P1 and N1.

6. Regarding claims 9-15, the combination of the Dingwall and Yamauchi et al. reference show all the recited limitations.

7. Claims 1-7, 9-18 and 21 are rejected under 35USC 103(a) as being unpatentable over Taylor (USP 5,644,255) in view of Yamauchi et al. (USP 6,373,321). Figure 2 of Taylor shows complementary source follower circuit comprising N and P channel transistors (203, 204) coupled in series between first and second power supply (Vcc and Vss), each transistor has a gate, source, drain and back gate terminal. Taylor does not show a back bias control circuit coupled to the back gate terminals of the transistors for controlling the threshold voltage of the transistors in active and standby modes as called for in claims 1 and 16. Figures 1A and AB of Yamauchi et al. show CMOS buffer circuit comprising P and N channel connected in series between a power supply and ground. The back gate of the P and N channel are controlled by a back bias control circuit (shown in figure 1c). The back bias control circuit supplies the back

gate terminal of the transistors with different bias potentials in active and standby mode thus varies the threshold voltage of the transistors accordingly. Specifically, the threshold voltage of the transistor is lowered in the active mode than in the standby mode to minimize the leakage current flow between source and the substrate thus reducing power consumption. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include the Yamauchi et al.'s back bias control circuit in the circuit arrangement of Taylor for controlling the threshold voltage of the N and P channel transistors thus reducing power consumption.

8. Regarding claims 2-6, 17-18 and 21, figures 2A-2B, 4 and 5 of Yamauchi et al. further teaches that CMOS transistor can also be fabricated in N, P or SOI substrates. The variations between these mythologies are well known in the art therefore the limitations of claims 2-6 and 17-18 will not be patentable under 35USC 103(a).

9. Regarding claim 7, the input signal applied to the combined source follower circuit of Taylor and Yamauchi can also an analog signal.

10. Regarding claims 9-15, the combination of the Dingwall and Yamauchi et al. reference show all the recited limitations.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (USP5,644,255) and Yamauchi et al. (USP 6,373,321). The combination of Taylor and Yamauchi et al. show all the limitations as noted above except for the level shifter for shifting the input signal before applied to the gate terminals of the N and P channel transistors as called for in claim 8. However, it is notoriously well known in the art that level shifter is commonly used to lower the input signal level thus to protect the gate terminals of the subsequent circuit

that receive the shifted input signal. Therefore, outside of any non-obvious results the obviousness of using a level shifter for lowering the input signal will not be patentable under 35USC 103(a).

12. Claims 1-7, 9-18 and 21 are rejected under 35USC 103(a) as being unpatentable over IBM-TDB volume 39, issue 6, pages 37-40) in view of Yamauchi et al. (USP 6,373,321). Figure 1B of IBM-TDB shows complementary source follower circuit comprising N and P channel transistors (T2, T1) coupled in series between first and second power supply (VDD and GND), each transistor has a gate, source, drain and back gate terminal. IBM-TDB does not show a back bias control circuit coupled to the back gate terminals of the transistors for controlling the threshold voltage of the transistors in active and standby modes as called for in claims 1 and 16. Figures 1A and AB of Yamauchi et al. show CMOS buffer circuit comprising P and N channel connected in series between a power supply and ground. The back gate of the P and N channel are controlled by a back bias control circuit (shown in figure 1c). The back bias control circuit supplies the back gate terminal of the transistors with different bias potentials in active and standby mode thus varies the threshold voltage of the transistors accordingly. Specifically, the threshold voltage of the transistor is lowered in the active mode than in the standby mode to minimize the leakage current flow between source and the substrate thus reducing power consumption. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include the Yamauchi et al.'s back bias control circuit in the circuit arrangement of the IBM-TDB for controlling the threshold voltage of the N and P channel transistors thus reducing power consumption.

13. Regarding claims 2-6, 17-18 and 21, figures 2A-2B, 4 and 5 of Yamauchi et al. further teaches that CMOS transistor can also be fabricated in N, P or SOI substrates. The variations between these mythologies are well known in the art therefore the limitations of claims 2-6 and 17-18 will not be patentable under 35USC 103(a).

14. Regarding claim 7, the input signal applied to the combined source follower circuit of IBM-TDB and Yamauchi can also an analog signal.

15. Regarding claims 9-15, the combination of the IMB-TDB and Yamauchi et al. reference show all the recited limitations.

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over IBM-TDB and Yamauchi et al. (USP 6,373,321). The combination of IBM-TDB and Yamauchi et al. show all the limitations as noted above except for the level shifter for shifting the input signal before applied to the gate terminals of the N and P channel transistors as called for in claim 8. However, it is notoriously well known in the art that level shifter is commonly used to lower the input signal level thus to protect the gate terminals of the subsequent circuit that receive the shifted input signal. Therefore, outside of any non-obvious results the obviousness of using a level shifter for lowering the input signal will not be patentable under 35USC 103(a).

17. Claims 1-7, 9-18 and 21 are rejected under 35USC 103(a) as being unpatentable over Japanese reference (JP 55-159604) in view of Yamauchi et al. (USP 6,373,321). Figure 4 of JP 55-159604 shows complementary source follower circuit comprising N and P channel transistors (Q1, Q2) coupled in series between first and second power supply (VDD and GND), each transistor has a gate, source, drain and back gate terminal. JP 55-159604 does not show a back bias control circuit coupled to the back gate terminals of the transistors for controlling the

threshold voltage of the transistors in active and standby modes as called for in claims 1 and 16. Figures 1A and AB of Yamauchi et al. show CMOS buffer circuit comprising P and N channel connected in series between a power supply and ground. The back gate of the P and N channel are controlled by a back bias control circuit (shown in figure 1c). The back bias control circuit supplies the back gate terminal of the transistors with different bias potentials in active and standby mode thus varies the threshold voltage of the transistors accordingly. Specifically, the threshold voltage of the transistor is lowered in the active mode than in the standby mode to minimize the leakage current flow between source and the substrate thus reducing power consumption. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include the Yamauchi et al.'s back bias control circuit in the circuit arrangement of the JP 55-159604 for controlling the threshold voltage of the N and P channel transistors thus reducing power consumption.

18. Regarding claims 2-6, 17-18 and 21, figures 2A-2B, 4 and 5 of Yamauchi et al. further teaches that CMOS transistor can also be fabricated in N, P or SOI substrates. The variations between these mythologies are well known in the art therefore the limitations of claims 2-6 and 17-18 will not be patentable under 35USC 103(a).

19. Regarding claim 7, the input signal applied to the combined source follower circuit of JP 55-159604 and Yamauchi can also an analog signal.

20. Regarding claims 9-15, the combination of the JP 55-159604 and Yamauchi et al. references show all the recited limitations.

21. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP 55-159604 and Yamauchi et al. (USP 6,373,321). The combination of JP 55-159-604 and Yamauchi et al. show

all the limitations as noted above except for the level shifter for shifting the input signal before applied to the gate terminals of the N and P channel transistors as called for in claim 8. However, it is notoriously well known in the art that level shifter is commonly used to lower the input signal level thus to protect the gate terminals of the subsequent circuit that receive the shifted input signal. Therefore, outside of any non-obvious results the obviousness of using a level shifter for lowering the input signal will not be patentable under 35USC 103(a).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 703-305-3791. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan T. Lam
Primary Examiner
Art Unit 2816

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December 19, 2003